

FORMAL DRAWINGS

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METHOD OF MANUFACTURING AN INTEGRATED
EDGE STRUCTURE FOR HIGH VOLTAGE
SEMICONDUCTOR DEVICES, AND RELATED
INTEGRATED EDGE STRUCTURE

By: Ferruccio Frisina
Express Mail Label No. EL844519516US

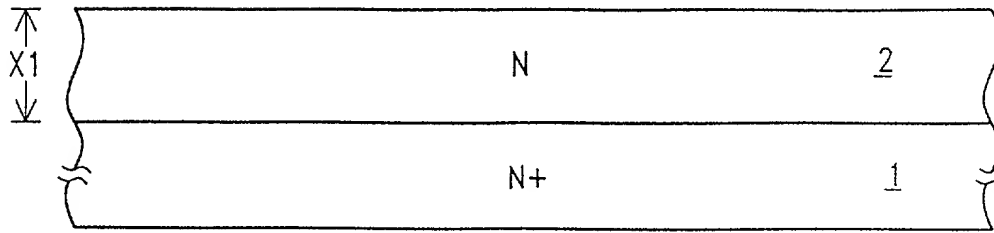


FIG. 1

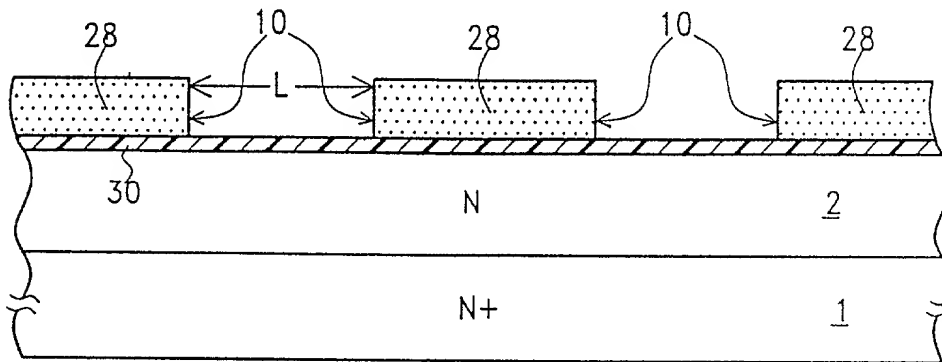


FIG. 2

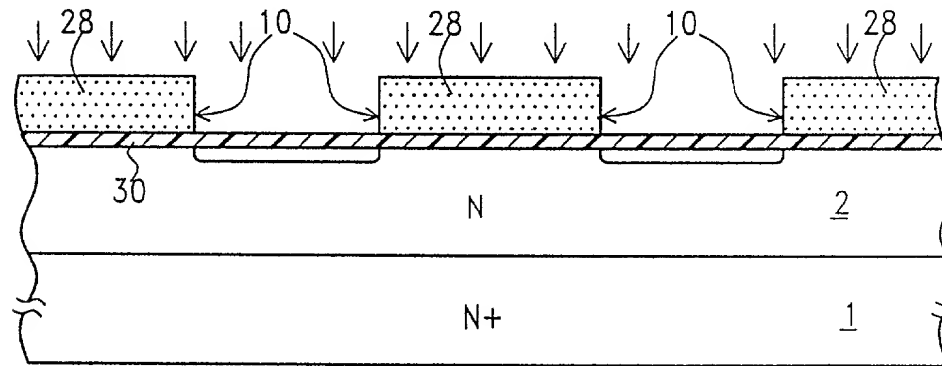


FIG. 3

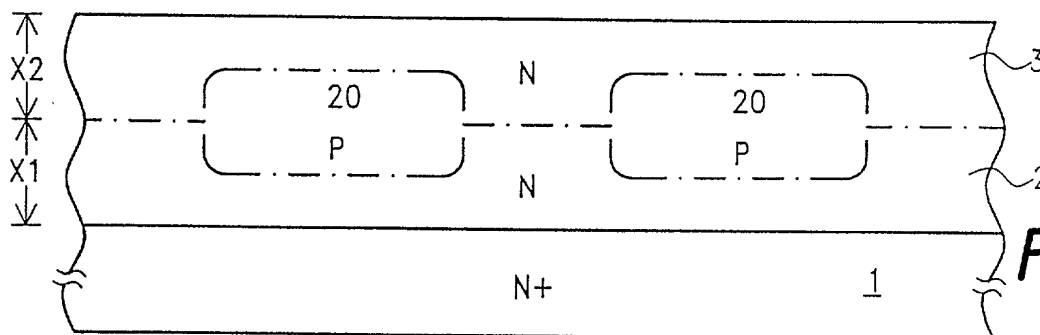


FIG. 4

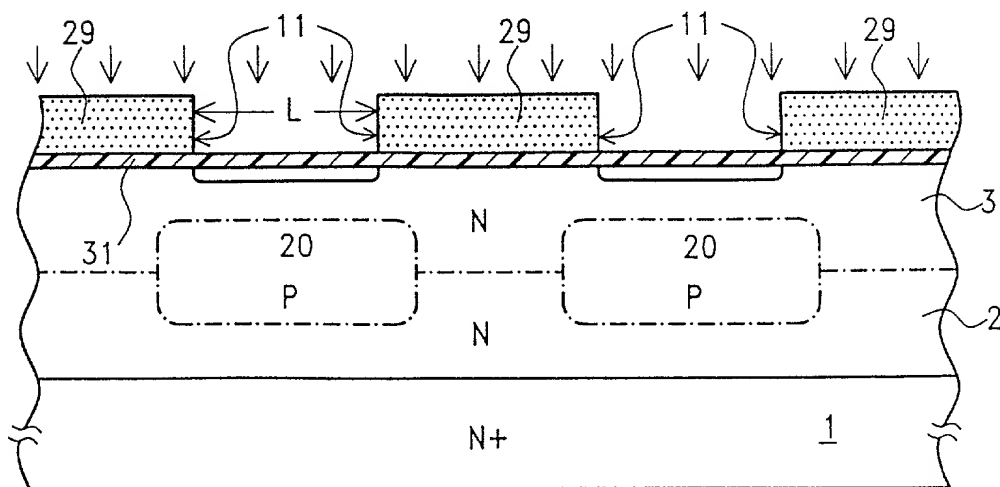


FIG. 5

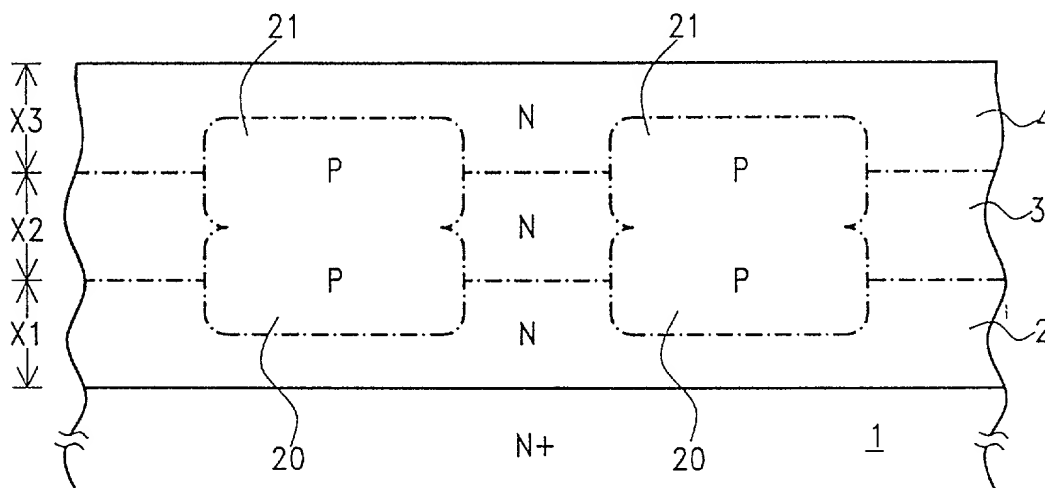


FIG. 6

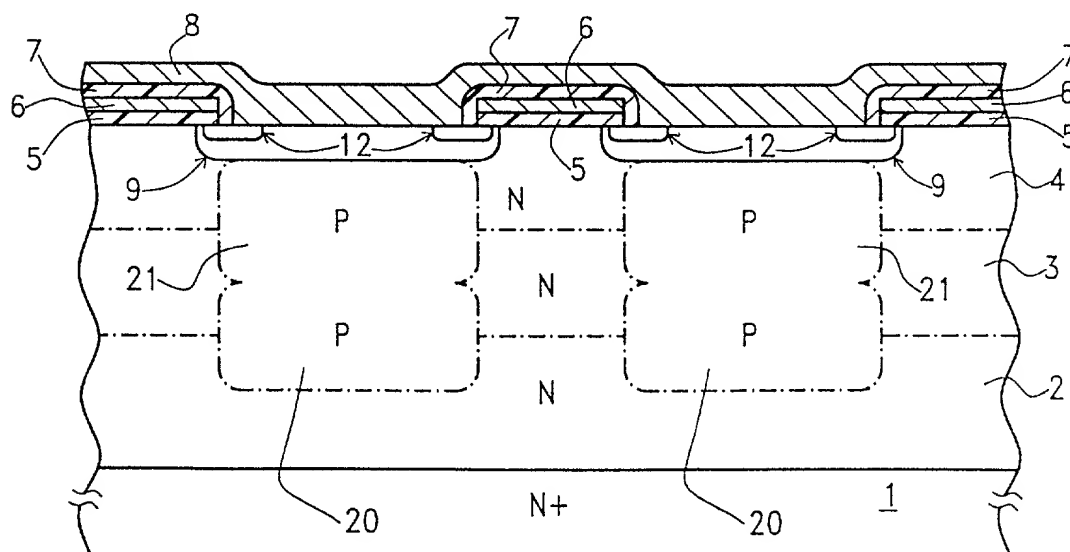


FIG. 7

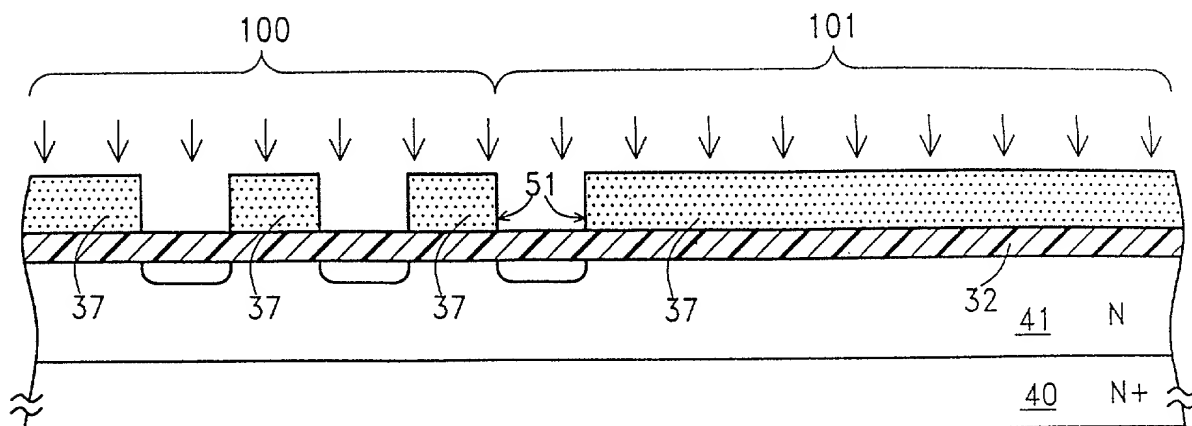


FIG. 8

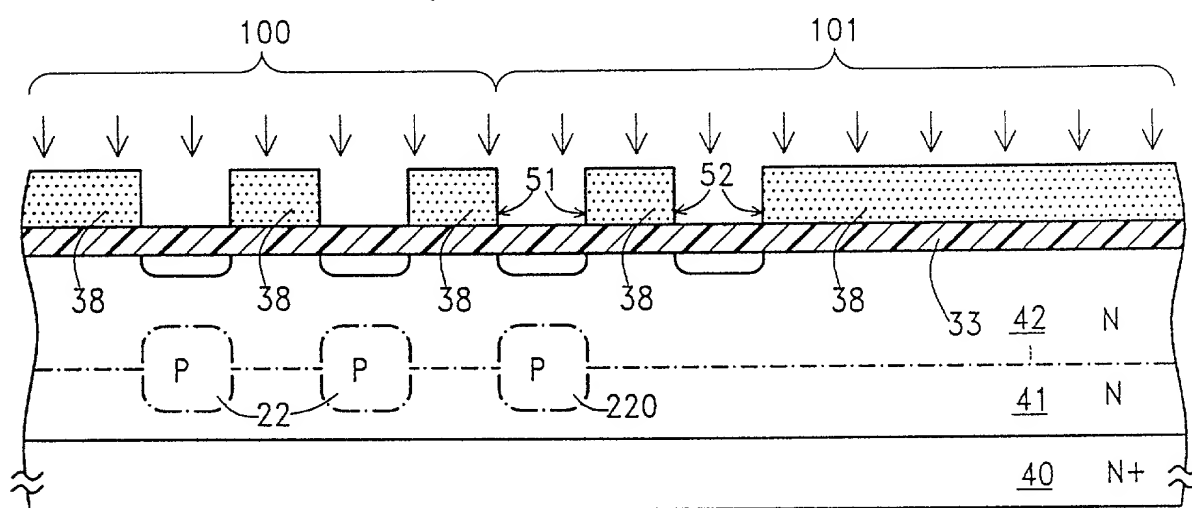


FIG. 9

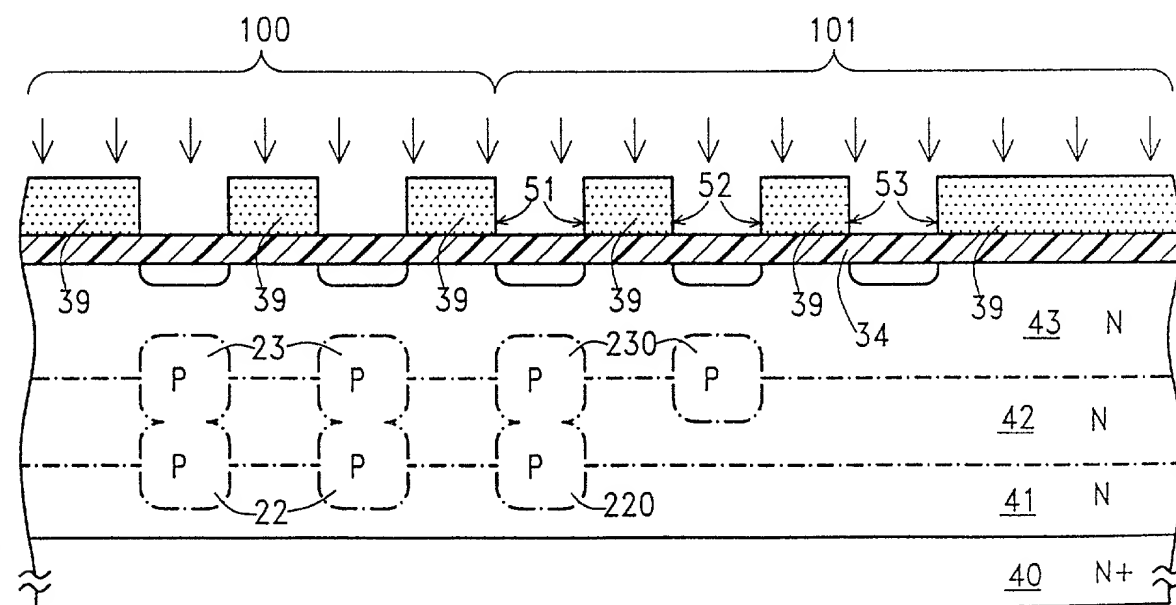


FIG. 10



FIG. 11

FIG. 12

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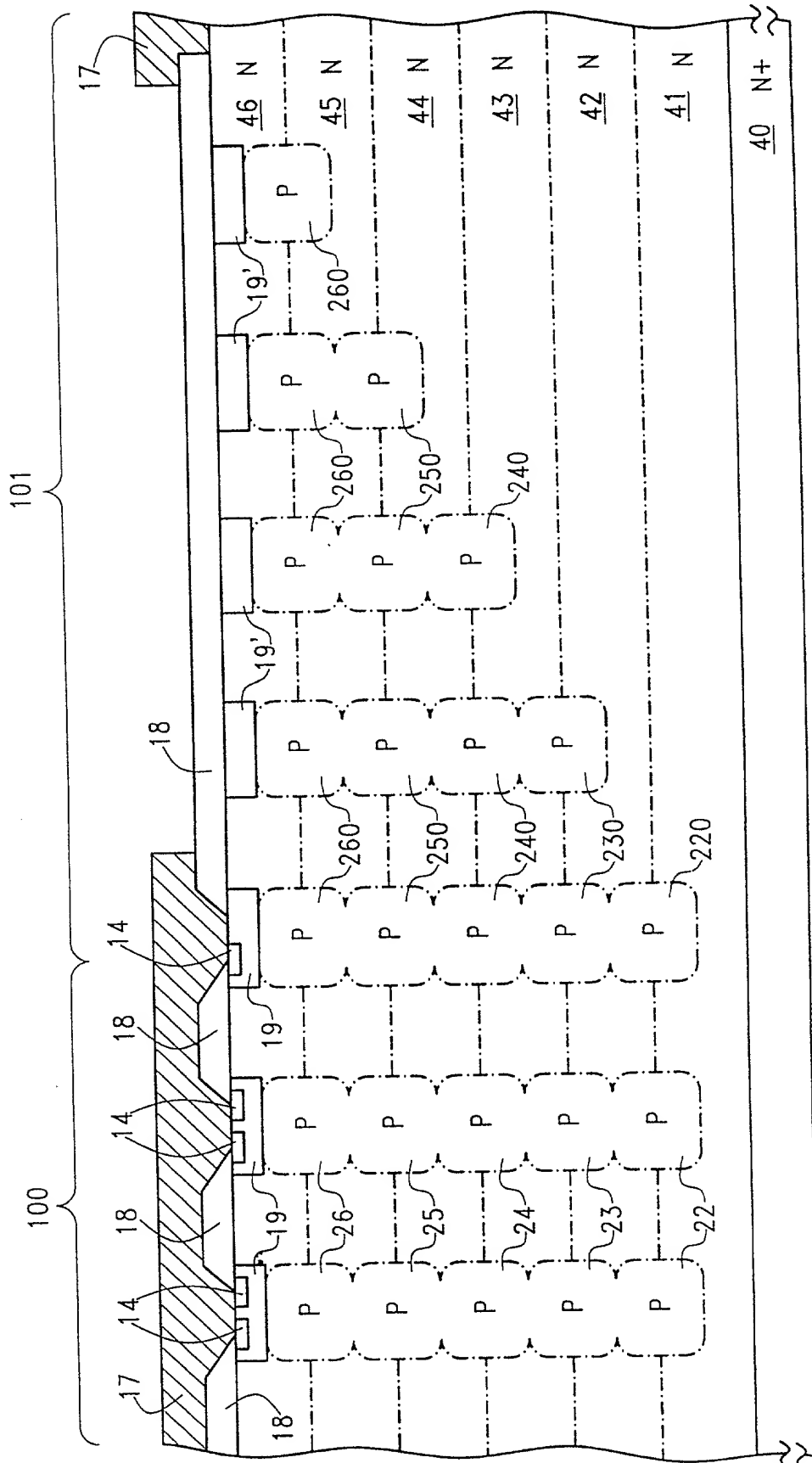


FIG. 12